

## AMENDMENT TO THE CLAIMS

### **Please amend the claims as follows:**

- 1 1. (previously presented) A memory system comprising:
  - 2 a first memory controller;
  - 3 a first memory component;
  - 4 a first address and control bus connected to the first memory controller and the first
  - 5 memory component, the first address and control bus including a plurality of
  - 6 signal conductors that extend from the first memory controller to the first
  - 7 memory component; and
  - 8 a first data bus connected to the first memory controller and to the first memory
  - 9 component, wherein the first data bus uses differential signaling and has a
  - 10 first data bus symbol time that is shorter than a first address and control bus
  - 11 symbol time of the first address and control bus.
  
- 1 2. (original) The memory system of claim 1 further comprising:
  - 2 a second memory component connected to the first address and control bus and to
  - 3 the first data bus.
  
- 1 3. (original) The memory system of claim 1 further comprising:
  - 2 a second memory component connected to the first address and
  - 3 control bus; and
  - 4 a second data bus connected to the first memory controller and to the second

5 memory component, wherein the second data bus uses differential signaling  
6 and has a second data bus symbol time that is shorter than the first address  
7 and control bus symbol time of the first address and control bus.

1 4. (original)The memory system of claim 1 wherein a quotient of the first data bus  
2 symbol time divided by the first address and control bus symbol time is less than or  
3 equal to 1/8.

1 5. (previously presented)A memory system comprising:  
2 a first memory controller;  
3 a first memory component;  
4 a first address and control bus connected to the first memory controller and to the  
5 first memory component, the first address and control bus including a  
6 plurality of signal conductors that extend from the first memory controller to  
7 the first memory component;  
8 a first clock signal conductor connected to the first memory controller and to the  
9 first memory component; and  
10 a first data bus connected to the first memory controller and to the first memory  
11 component, wherein the first data bus has a first data bus symbol time that is  
12 shorter than a first address and control bus symbol time of the first address  
13 and control bus and wherein the first address and control bus symbol time is  
14 shorter than a first clock signal cycle time of the first clock signal.

1 6. (original) The memory system of claim 5 further comprising:  
2 a second memory component connected to the first address and control bus, to the

3 first clock signal conductor, and to the first data bus.

1 7. (original) The memory system of claim 5 further comprising:

2 a second memory component connected to the first address and control bus and to  
3 the first clock signal conductor; and

4 a second data bus connected to the first memory controller and to the second  
5 memory component, wherein the second data bus uses differential signaling  
6 and has a second data bus symbol time that is shorter than the first address  
7 and control bus symbol time of the first address and control bus.

1 8. (original) The memory system of claim 5 wherein a first quotient of the first data  
2 bus symbol time divided by the first address and control bus symbol time is less  
3 than or equal to  $1/8$  and a second quotient of the first address and control bus  
4 symbol time divided by the first clock signal cycle time is less than or equal to  $1/2$ .

1 9. (previously presented) A memory system comprising:

2 a first memory controller;

3 a first memory component;

4 a first address and control bus connected to the first memory controller and to the  
5 first memory component, the first address and control bus including a  
6 plurality of signal conductors that extend from the first memory controller to  
7 the first memory component; and

8 a first data bus connected to the first memory controller and to the first memory  
9 component, wherein the first memory component includes a first termination  
10 structure connected to the first data bus and wherein the first data bus has a

- 11 first data bus symbol time that is shorter than a first address and control  
12 symbol time of the first address and control bus.
- 1 10. (original) The memory system of claim 9 further comprising:  
2 a second memory component connected to the first address and control bus; and  
3 a second data bus connected to the first memory controller and to the second  
4 memory component, wherein the second memory component includes a  
5 second termination structure connected to the second data bus and wherein the  
6 first data bus symbol time is shorter than the first address and control bus  
7 symbol time of the first address and control bus.
- 1 11. (original) The memory system of claim 9 wherein the first memory controller  
2 includes a third termination structure connected to the first data bus.
- 1 12. (original)The memory system of claim 9 wherein a quotient of the first data bus  
2 symbol time divided by the first address and control bus symbol time is less than or  
3 equal to 1/8.
- 1 13. (original)The memory system of claim 9 wherein a calibration process is used to  
2 adjust a first termination value of the first termination structure.
- 1 14. (Previously presented)A memory system comprising:  
2 a first memory controller;  
3 a first memory component;  
4 a first address and control bus connected to the first memory controller and to the

5 first memory component, the first address and control bus including a  
6 plurality of signal conductors that extend from the first memory controller to  
7 the first memory component; and  
8 a first data bus connected to the first memory controller and to the first memory  
9 component, wherein the first memory component includes a first termination  
10 structure connected to the first data bus, wherein the first data bus uses  
11 differential signaling, and wherein the first address and control bus uses non-  
12 differential signaling.

1 15. (original) The memory system of claim 14 further comprising:  
2 a second memory component connected to the first address and control bus; and  
3 a second data bus connected to the first memory controller and to the second  
4 memory component, wherein the second memory component includes a  
5 second termination structure connected to the second data bus and wherein the  
6 second data bus uses differential signaling.

1 16. (original) The memory system of claim 14 wherein the first memory controller  
2 includes a third termination structure connected to the first data bus.

1 17. (original) The memory system of claim 14 wherein a calibration process is used to  
2 adjust a first termination value of the first termination structure.

1 18. (previously presented) A memory system comprising:  
2 a first memory controller;  
3 a first memory component;

4 a first address and control bus connected to the first memory controller and to the  
5 first memory component, the first address and control bus including a  
6 plurality of signal conductors that extend from the first memory controller to  
7 the first memory component; and  
8 a first data bus connected to the first memory controller and to the first memory  
9 component, wherein the first data bus uses differential signaling and wherein  
10 the first memory component accesses a first word stored in the first memory  
11 component, the first word being wider than a first data bus width of the first  
12 data bus.

1 19. (original) The memory system of claim 18 further comprising:  
2 a second memory component connected to the first address and control bus and to  
3 the first data bus.

1 20. (original) The memory system of claim 18 further comprising:  
2 a second memory component connected to the first address and control bus; and a  
3 second data bus connected to the first memory controller and to the second  
4 memory component, wherein the second data bus uses differential signaling  
5 and wherein the second memory component accesses a second word stored in  
6 the second memory component, the second word being wider than a second  
7 data bus width of the second data bus.

1 21. (currently amended) A memory system comprising:  
2 a first memory controller;  
3 a first memory component;

4 a first address and control bus connected to the first memory controller and to the  
5 first memory component, the first address and control bus including a  
6 plurality of signal conductors that extend ~~from~~ from the first memory  
7 controller to the first memory component; and  
8 a first data bus connected to the first memory controller and to the first memory  
9 component, wherein the first memory controller includes a first receive circuit  
10 having a first read timing adjustment subcircuit for adjusting a first adjustable  
11 read data sampling time point for first read data sampled from the first data  
12 bus and wherein the first data bus uses differential signaling.

1 22. (original) The memory system of claim 21 further comprising:  
2 a second memory component connected to the first address and control bus; and  
3 a second data bus connected the first memory controller and to the second memory  
4 component, wherein the first memory controller includes a second receive  
5 circuit having a second read timing adjustment subcircuit for adjusting a  
6 second adjustable read data sampling time point for second read data sampled  
7 from the second data bus and wherein the second data bus uses differential  
8 signaling.

1 23. (original) The memory system of claim 21 wherein a calibration process is used to  
2 adjust the first adjustable read data sampling time point.

1 24. (original) The memory system of claim 21 wherein the first memory controller  
2 contains a first transmit circuit having a first write timing adjustment subcircuit for  
3 adjusting a first adjustable write data driving time point for first write data driven

4 on the first data bus.

1 25. (Currently Amended) A memory system comprising:

2 a first memory controller;

3 a first memory component;

4 a first address and control bus connected to the first memory controller and to the

5 first memory component, the first address and control bus including a

6 plurality of signal conductors that extend ~~from~~ from the first memory

7 controller to the first memory component; and

8 a first data bus connected to the first memory controller and to the first memory

9 component, wherein the first memory controller component includes a first

10 receive circuit having a first read timing adjustment subcircuit for adjusting a

11 first adjustable read data sampling time point for first read data sampled from

12 the first data bus and wherein the first memory component includes a first

13 termination structure connected to the first data bus.

1 26. (original) The memory system of claim 25 further comprising:

2 a second memory component connected to the first address and control bus; and

3 a second data bus connected to the first memory controller and to the second

4 memory component, wherein the first memory controller includes a second

5 receive circuit having a second read timing adjustment subcircuit for adjusting

6 a second adjustable read data sampling time point for second read data

7 sampled from the second data bus and wherein the second memory

8 component includes a second termination structure connected to the second



9 data bus.

1 27. (original) The memory system of claim 25 wherein a calibration process is used to  
2 adjust the first adjustable read data sampling time point.

1 28. (original) The memory system of claim 25 wherein the first memory controller  
2 includes a first transmit circuit having a first write timing adjustment subcircuit for  
3 adjusting a first adjustable write data driving time point for first write data driven  
4 on the first data bus.

1 29. (original) The memory system of claim 25 wherein the first memory controller  
2 includes a third termination structure connected to the first data bus.

1 30. (previously presented)The memory system of claim 1 further comprising a memory  
2 module having the first memory component disposed thereon, and wherein the  
3 plurality of signal conductors include, at least in part, conductive traces disposed on  
4 the memory module.

1 31. (previously presented)The memory system of claim 5 further comprising a memory  
2 module having the first memory component disposed thereon, and wherein the  
3 plurality of signal conductors include, at least in part, conductive traces disposed on  
4 the memory module.

1 32. (previously presented)The memory system of claim 9 further comprising a memory  
2 module having the first memory component disposed thereon, and wherein the  
3 plurality of signal conductors include, at least in part, conductive traces disposed on

4 the memory module.

1 33. (previously presented)The memory system of claim 14 further comprising a  
2 memory module having the first memory component disposed thereon, and wherein  
3 the plurality of signal conductors include, at least in part, conductive traces  
4 disposed on the memory module.

1 34. (previously presented)The memory system of claim 18 further comprising a  
2 memory module having the first memory component disposed thereon, and wherein  
3 the plurality of signal conductors include, at least in part, conductive traces  
4 disposed on the memory module.

1 35. (previously presented)The memory system of claim 21 further comprising a  
2 memory module having the first memory component disposed thereon, and wherein  
3 the plurality of signal conductors include, at least in part, conductive traces  
4 disposed on the memory module.

1 36. (previously presented)The memory system of claim 25 further comprising a  
2 memory module having the first memory component disposed thereon, and wherein  
3 the plurality of signal conductors include, at least in part, conductive traces  
4 disposed on the memory module